**Remarks:**

The present response is intended to be fully responsive to all points raised by the Examiner and is believed to place the application in condition for allowance. Allowance of the application is respectfully requested.

**Status of Claims**

Claims 1 – 6 are pending in the application. Claims 1 – 6 are rejected. Claims 3 – 6 have been amended. New claims 7 and 8 have been added. Applicants respectfully submit that the amendments to claims 3 – 6 and new claims 7 – 8 do not add new matter.

**Claim Rejections – 35 USC 102**

Claims 3 – 6 are rejected under 35 USC 102(b) as being anticipated by US Patent No. 3,673,399 (Hancke et al.). Applicant respectfully traverses this rejection, in view of the remarks that follow.

As is well established, in order to successfully assert a *prima facie* case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected.

According to Hancke et al., the operands for Pass 1 of the Fast Fourier Transform (FFT) are read from input buffer memory 60 (Fig. 6), which is part of input buffer 23 (Fig. 1). After Pass 1 of the FFT is performed by arithmetic unit (AU) 21, the calculated operands (which are the operands of Pass 2) are stored in output buffers 24 and 25. This is evident from the following passage: "During Pass 1, of the processing mode, data is read from input buffer memory 60. ... After each read operation from input buffer memory 60 the operands $B_r$ and $C_r$ are clocked into the AU 21 where the first set of operands $A_r$ and $A_{r+n/2}$ are computed. The computed operands $A_r$ and $A_{r+n/2}$ are then gated through output switch gates 28 and placed in output buffers 24 and 25, as shown in Table II." (col. 10, lines 30-49)

In particular, in Pass 1, the computer operands $A_r$ and $A_{r+n/2}$ are not stored in the memory space from which the operands $B_r$ and $C_r$ were fetched, i.e. are not stored in input buffer 60.

Therefore, Hancke et al. does not teach, either expressly or inherently, the following limitation of amended claim 3: *"storing a first output data point of said initial stage at said*

*first address in said first memory space and a second output data point of said initial stage at said second address"* where *"said first address"* refers to the address in the first memory space *"where a first data point of a pair of input data points of* ***an initial stage*** *of a Fast Fourier Transform calculation is stored"* and *"said second address"* refers to the address in the second memory space *"where a second data point of said is stored"*. Accordingly, Hancke et al. cannot anticipate claim 3 as amended. Since claim 4 is dependent from claim 3 and includes all the limitations of the independent claim, Hancke et al. cannot anticipate claim 4.

Moreover, Hancke et al. does not teach, either expressly or inherently, the following limitation of amended claim 5: *"determining ... whether to store an output data point of* ***an initial stage*** *of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address, where a first data point of a pair of input data points of said initial stage is stored in said first memory space at said first address and a second data point of said pair is stored in said second memory space at said second address, and where said first address and said second address both correspond to said memory index"*. Hancke et al. does not store the output data points of Pass 1 in input buffer 23. Rather Hancke et al. determines whether to store the output data points in buffer 24 or buffer 25. Accordingly, Hancke et al. cannot anticipate claim 5 as amended.

For similar reasons, Hancke et al. does not teach, either expressly or inherently, the following limitation of amended claim 6: *"means for determining ... whether to store an output data point* ***of said initial stage*** *in said first memory space at said first address or in said second memory space at said second address"*, where *"said first address"* refers to the address in the first memory space where *"a first data point of a pair of input data points* ***of an initial stage"*** are stored and where *"said second address"* refers to the address in the second memory space where *"a second data point of said pair"* are stored. Accordingly, Hancke et al. cannot anticipate claim 6 as amended.

**Claim Rejections – 35 USC 103**

Claims 1 – 6 are rejected under 35 USC 103(a) as being unpatentable over Hancke et al. in view of US Patent No. 3,871,577 (Avellar et al.). Applicant respectfully traverses this rejection, in view of the remarks that follow.

On page 5 of the Office Action, the Examiner stated "the main different between the reference and the present application is the initial stage wherein all the input data points are stored in the first and second memory storage prior the first stage FFT operation in the present application and the input data points are stored temporarily in a third memory storage, passed through first stage of FFT operation, than stored in the first and second memory storage in the reference."

Applicants strongly disagree with this statement. There are many significant differences between the claimed invention and Hancke et al., as explained in Applicants' remarks regarding Hancke et al.

Specifically regarding claim 1, claim 1 recites *"for each FFT stage 0 data point grouping comprising a first data point ... in said first memory space X and a corresponding second data point ... in said second memory space Y"* that *"a parity of a data point memory index"* is determined, and based on the value of that parity, *"the results of an FFT operation upon said first data point"* are stored either *"at the memory address in said first memory space X from which said first data point was fetched"* or *"at the memory address in said second memory space Y from which said second data point was fetched"*. Hancke et al. fails to teach or suggest these limitations, since for Pass 1 (the equivalent of FFT stage 0), the data points (operands) are read from input buffer memory 60 (Fig. 6), which is part of input buffer 23 (Fig. 1), and the results are stored buffer 24 and buffer 25, not at the memory address from which the operands were fetched.

Avellar et al. fails to cure the deficiencies of Hancke et al. "Referring now to FIG. 1, reference numerals 10 and 12 represent, for example, input buffers for storing N/2 complex data points or samples each ... during one half $(t_1/2)_a$ of the first pass $t_1$ data points 0 and 4 are respectively fed to ... memory 16 ... during the next half $(t_1/2)_b$ of the first pass interval, the output data from the arithmetic unit 14 is switched to the memory 18." (col. 3, lines 36 – 63) Clearly Avellar et al. does not teach or suggest the above-quoted limitation of claim 1, since the output of the first pass is stored in different memories than the input buffers.

Accordingly, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest all the limitations of claim 1. Claim 2 is dependent from claim 1 and includes all

the limitations of the independent claim. Consequently, the Office Action has failed to establish a *prima facie* case of obviousness for claims 1 and 2.

Regarding claims 3 – 6, the Examiner has failed to give any reasons why these claims are unpatentable over Hancke et al. in view of Avellar et al. The burden to respond to the rejection of claims 3 – 6 under 35 USC 103(a) does not fall on the Applicants until the Examiner establishes a prima facie case for obviousness. However, in the interest of advancing this application to issue, Applicants have prepared the following remarks.

Claims 3 – 6 have been amended and Applicants have presented remarks above explaining why Hancke et al. fails to anticipate claims 3 – 6 as amended. Avellar et al. fails to cure the deficiencies of Hancke et al. as explained above in the remarks regarding claims 1 and 2. Accordingly, Hancke et al. and Avellar et al., alone and in combination, fail to teach or suggest all the limitations of claims 3 – 6.

**Remarks to cited references**

37 CFR 1.111(c) requires an Applicant to clearly point out the patentable novelty which Applicant thinks the newly added claims present in view of the state of the art disclosed by the references cited. According to MPEP 714.02 and 714.04, Applicant is to clearly point out the patentable novelty of a newly added claim by specifically pointing out how the language of the claim patentably distinguishes the claim from the references cited, in order to provide a complete prosecution record as to why the claim should be allowed over the prior art of record. Applicants have presented such arguments below.

Remarks to new Claim 7

Hancke et al. discloses "The computed outputs from the simultaneous calculations of the arithmetic unit are stored in and retrieved from a pair of memory buffers on an "in-place" basis. ... A parity check of the binary counter output serves to route the computed operands to the correct buffer memory." (col. 1, line 72 – col. 2, line 6) However, the address in the buffer memory where the computed operands are stored according to Hancke et al. is not "the sum of a first base address and said memory index" or "the sum of a second base address and said memory index", where the memory index is the number whose parity is being checked.

Avellar et al. does not perform in-place memory management.

Therefore, Hancke et al. and Avellar et al., alone or in combination, fail to teach or suggest the following limitation of claim 7: *"if said parity is of a first parity value, storing a first output data point of said stage at said first address in said first memory space and a second output data point of said stage at said second address in said second memory space"* where *"said parity"*, *"said first address"* and *"said second address"* refer to *"a parity of a memory index, where a first data point of a pair of input data points of a stage of a Fast Fourier Transform calculation is stored in a first memory space at a first address that is the sum of a first base address and said memory index, and a second data point of said pair is stored in a second memory space at a second address that is the sum of a second base address and said memory index"*.

Remarks to new Claim 8

The remarks regarding Hancke et al. and Avellar et al. given above with respect to claim 7 are applicable here too.

Therefore, Hancke et al. and Avellar et al., alone or in combination, fail to teach or suggest the following limitation of claim 8 *"determining, based at least on a parity of a memory index, whether to store an output data point of a stage of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address"*, where the first address is the sum of a first base address and the memory index and the second address is the sum of a second base address and the memory index.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

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